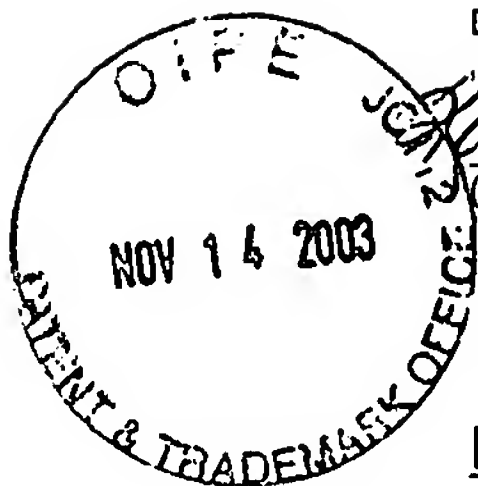


I hereby certify that this correspondence is being deposited with the United States Postal Service as in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313, on November 12, 2003. The applicant and/or attorney requests the date of deposit as the filing date.
Depositor: Karen Cing-Mars



Karen Cing-Mars 11/12/03
(Signature & date)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of _____: November 12, 2003
Michael P. Belyansky et al.: Group Art Unit:
Serial No. 10/605,857 : Examiner:
Filed: 10/31/2003 : International Business Machines Corporation
2070 Route 52
Hopewell Junction, NY 12533

TITLE: HDP Process for High Aspect Ratio Gap Filling

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

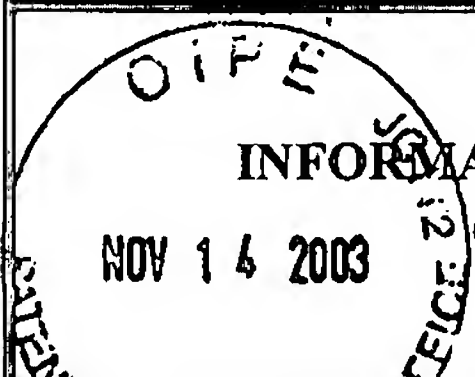
Pursuant to the duty of disclosure set forth in 37 C.F.R. 1.56, and further pursuant to the provisions of 37 C.F.R. 1.97 and 1.98, applicants hereby respectfully submit copies of the prior patents and publications as listed on Form PTO-1449, attached hereto.

In citing these documents, no representation is made nor intended as to the pertinency or non-pertinency of the art, that better art than that listed is not available, or that other art is not applicable.

Respectfully submitted,
Michael P. Belyansky et al.

BY

Steven Capella, Attorney
Registration No. 33,086
Telephone No. 845-894-3669

<div style="text-align: center;">  <p>INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)</p> </div>	Docket Number (Optional) FIS920030085US1	Application Number 10/605,857
	Applicant(s) Michael P. Belyansky et al.	
	Filing Date October 31, 2003	Group Art Unit

U.S. PATENT DOCUMENTS							
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS								
	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>		
		High-Density Plasma Chemical Vapor Deposition of Silicon-Based Dielectric Films for Integrated Circuits, S.V. Nguyen; IBM Journal of Research and Development, Volume 43, 1/2, 1999, Plasma Processing

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.